

501.25958CV7  
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: T. HOTTA, et al

Serial No.: Not yet assigned

Filing Date: November 6, 2003

For: DATA PROCESSING SYSTEM GENERATING CLOCK SIGNAL  
FROM AN INPUT CLOCK PHASE LOCKED TO THE INPUT CLOCK  
AND USED FOR CLOCKING LOGIC DEVICES

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR §1.97 & 1.98**

**MS DD**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

November 6, 2003

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR §1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. §120."

Applicant(s) are submitting herewith a copy of Form PTO-1449 which list documents cited in parent application(s) Serial No. 10/002,444, filed December 6, 2001, which is a continuation of application Serial No. 09/406,921, filed September 28, 1999, now abandoned; which is a continuation of application Serial No. 08/788,831, filed January 27, 1997, now U.S. Patent No. 5,974,560; which is a

continuation of Serial No. 08/279,887, filed July 26, 1994, now U.S. Patent No. 5,640,547; which is a divisional of Serial No. 07/872,174, filed April 22, 1992, now U.S. Patent No. 5,388,249; which is a continuation of Serial No. 07/184,782, filed April 22, 1988, now U.S. Patent No. 5,133,064; and is related to application Serial No. 08/278,245, filed July 21, 1994, now U.S. Patent No. 5,506,982; and application Serial No. 08/460,601, filed June 2, 1995, now U.S. Patent No. 5,542,083.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (501.25958CV7) please credit any excess fees to such deposit account.

Respectfully submitted,



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CIB/jdc  
(703) 312-6600

**FORM PTO-1449** U.S. Department of  
Commerce (Rev. 4/92) Patent and Trademark  
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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use several sheets if necessary)

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November 6, 2003GROUP  
2185

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING D. IF APPROP.										
						4	6	6	1	7	2	1	4/87	Ushiku	307	269
	4 7 6 1 5 6 5	8/88	Kannagundla	307	243											
	4 9 5 8 0 9 2	9/90	Tanaka	307	480											
	5 4 5 1 8 9 2	9/95	Bailey	327	113											10/3/94
	4 6 8 9 5 8 1	8/87	Talbot	331	1A											7/3185
	3 9 4 0 5 5 8	2/76	Gabbard	375	356											
	4 8 2 3 2 6 2	4/89	Calle	395	550											6/26/87
	4 6 9 2 9 3 2	9/87	Denhez	375	356											2/6/86
	4 6 8 0 7 7 9	7/87	Wakerly	375	356											1/14/85
	4 5 1 9 0 7 1	5/85	Miller	370	105.3											
	4 6 3 9 8 5 6	1/87	Hristich	395	575											11/4/83

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT	
						YES	NO
	0 1 1 3 5 1 6	7/84	European				

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

	Kazuo Kato, et al, "A Low-Power 128 MHZ VCO for Monolithic PLL IC's" IEEE Journal of Solid State Circuits, 1988, vol. 23, No. 2, pp. 474-479.
	Deog-Kyoun-Jeong, "Design of PLL-Based Clock Generation Circuits", IEEE Journal of Solid State Circuits, 1987, vol. SC-22, No. 2, pp. 255-261.
	"A Synchronous Approach for Clocking VLSI Systems", IEEE Journal of Solid State Circuits, February 1982, SC-17, No. 1, pp. 51-56.

EXAMINER	DATE CONSIDERED

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	5 0 9 5 4 2 5	3/92	Hesse	395	550	1/9/85
	4 8 9 0 2 2 2	12/89	Kirk	395	550	12/17/8
	4 5 9 0 4 3 9	5/89	Goggin	331	60	5/7/84
	4 8 4 7 5 1 6	7/89	Fujita	307	269	11/23/8
	3 7 5 8 7 2 0	9/73	Dinn	307	269	
	3 8 2 9 7 9 0	8/74	Macrander	331	61	
	4 8 9 3 2 7 1	1/90	Davis	364	900	11/7/83
	4 4 6 8 6 3 4	8/84	Takagi	331	60	
	3 9 6 1 2 6 9	6176	Alvarez	331	60	
	4 5 2 1 8 9 3	6/85	Bellman	331	60	
	4 9 0 6 9 4 4	3190	Frerking	31	1A	8/11/88

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						YES

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

	"A 130 k-Gate CMOS Mainframe Chip Sets", ISSCC, Session VIII, pp. 86-87.
	"A ISMIPS 326 Microprocessors", ISSCC, Session II, 1987, pp. 26-27.
	"A Low-Power 128-MHz VCO for Monolithic PLL1C's", K. Kato, IEEE Journal of Solid-State Circuits, vol. 23, April 1988, pp. 474-479.

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		4	8	2	9	5	4	5					
	4 8 6 2 1 0 4	5/89	Guzik	331	1A	8/25/86							
	4 8 6 2 1 0 4	8/89	Muratani	331	1A	4/6/88							
	4 8 6 4 2 5 3	9/89	Zwack	331	1A	9/21/88							
	4 7 7 9 0 0 8	10/88	Kessels	331	1A	10/11/88							
	4 6 7 3 8 9 1	6/87	Remy	331	2								
	4 4 8 6 8 5 0	12/84	Hyatt	364	747								
	4 6 3 0 1 9 3	12/86	Kris	364	200	9/23/86							
	4 6 4 4 4 9 8	2/87	Bedard	364	900	9/26/86							
	4 5 0 4 7 4 5	3/85	Spence	307	270								
	4 7 5 4 1 6 4	6/88	Flora	307	269	6/30/86							
	4 6 7 7 3 9 4	6/87	Vollmer	331	1A	6/21/86							

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	<b>APPLICANT</b> <b>HOTTA, et al</b>	
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## **U.S. PATENT DOCUMENTS**

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